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RESEARCH STUDY INTO THE NEAR EARTH APPLICATION OF MILLIMETER RADIO WAVES AS APPLIED TO CERTAIN BATTLEFIELD PROBLEMS

John M Cotton, Jr

Advanced Technology Corporation
Timonium, Maryland

December 1967

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Special Technical Report
on
Work Assignment #5

ADVANCED TECHNOLOGY CORPORATION
1830 York Road
Timonium, Maryland

JAN 19 1968

December 15, 1967

Ballistic Research Laboratories
Aberdeen Proving Ground, Maryland

Contract No. DA-18-001-AMC-829(X)

ADVANCED TECHNOLOGY CORPORATION
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ABSTRACT

This report describes the design of a 35 GHz solid state source. A unique feature of the source is a linear FM capability of 350 MHz at sweep rates from 5 Hz to greater than 20 kHz. The output power is approximately 50 mW. Frequency stability is derived from an 81 MHz crystal controlled oscillator. Transistor circuitry brings this signal up to 324 MHz at 9 watts. A varactor multiplier chain then is used to achieve the final output frequency.

This source was developed as one of several work assignments of the subject contract.

1. INTRODUCTION

The report which follows describes the final design and performance characteristics of a 35 GHz solid state source with FM capability. At the outset of the development, performance specifications were delineated on a best effort basis. It was agreed that the source was to be a crystal controlled oscillator followed by a multiplier chain. The FM capability was to be 1% or greater with an output amplitude variation of less than 10% over this range. The FM should be achieved by driving the unit with no more than a one volt signal in the 5 Hz to 20 kHz frequency range. The output power was to be 25 mW minimum with a frequency stability of at least 1 part in 10^5.

In the delivered source, all of these goals were achieved or exceeded. This report will not presume to detail every step of the development process. Rather we shall describe here simply the designs which were finally selected to fabricate the finished product.

2. OSCILLATOR, CONTROL AND DRIVER CIRCUITRY

The block diagram of Figure 1 outlines the manner in which the first half of the source was assembled and will be the focal point of the discussion which follows. The complete circuit diagrams which "open up" these blocks will be referenced in the text but included following the description.

The basic frequency source is an 81.000 MHz crystal controlled oscillator (Figure 2), which provides the reference signal at all times. The oscillator which actually furnishes signal to the driver and subsequent multiplier stages is a voltage controlled oscillator (Figure 3), which has the capability of a one percent linear FM deviation. The average frequency of this VCO is locked to the crystal oscillator through an AFC circuit. Since it was required that the FM capability extend down to a 5 Hz rate, the response time of this AFC loop must be made long compared to 5 Hz. This was accomplished in the following manner (See Figure 4).

An astable multivibrator operating at a 0.5 Hz rate is used to generate the gating signal. Signal from the reference oscillator is then amplified in a buffer stage for isolation and brought to one of the switches, or gates (Figure 5). A sample of the VCO signal is also passed through buffer amplifier isolating stages and applied to the other gate. (An attenuator was included in this path to provide for amplitude adjustment to a level equal to the reference signal.) The gates then sequentially pass the VCO and the reference signals to a limiter and discriminator circuit (Figure 6). Any difference frequency which exists between the one second average of the VCO and the pure frequency of the crystal oscillator will produce a square wave at the output of the discriminator. The amplitude of this square wave will of course be proportional to the frequency. The phase of the square wave will determine the direction of the VCO drift.

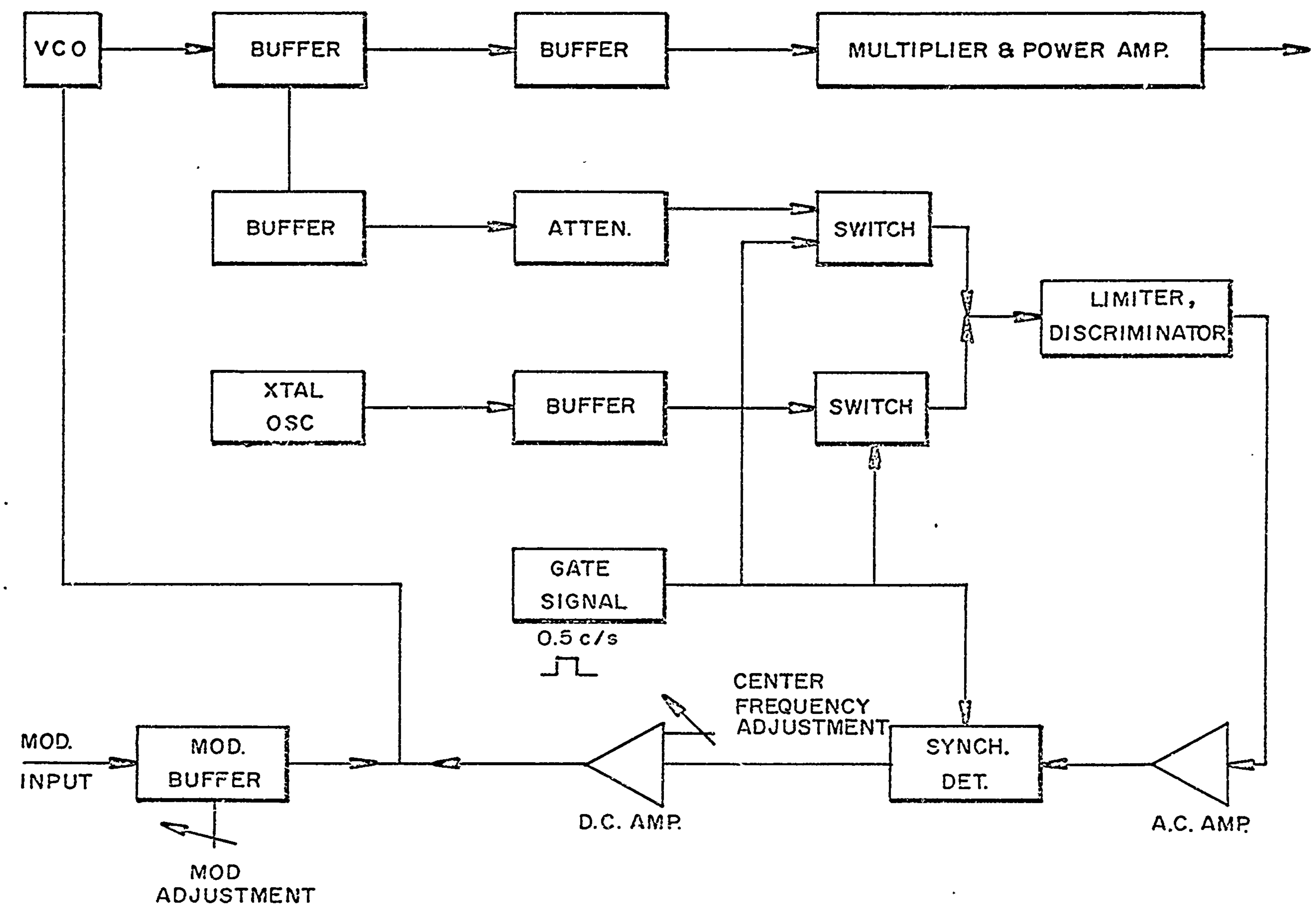

FIG. I BLOCK DIAGRAM OF OSCILLATOR, CONTROL AND DRIVER CIRCUITS

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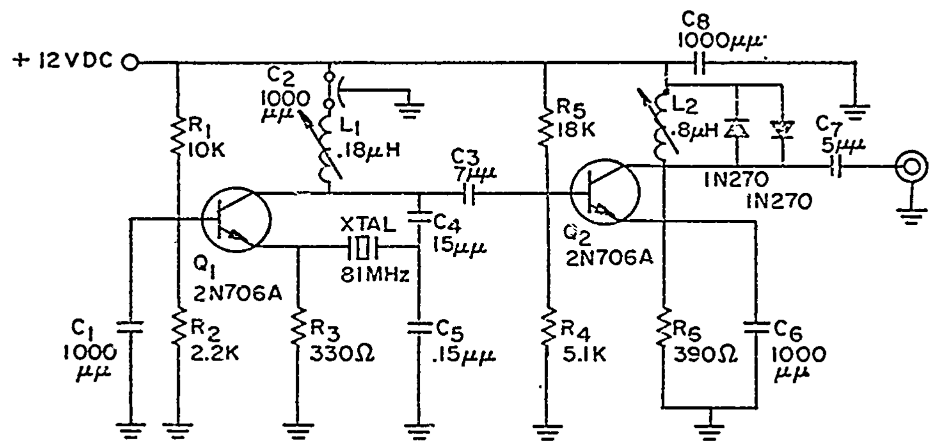

FIG. 2 – 81 MHz OSCILLATOR

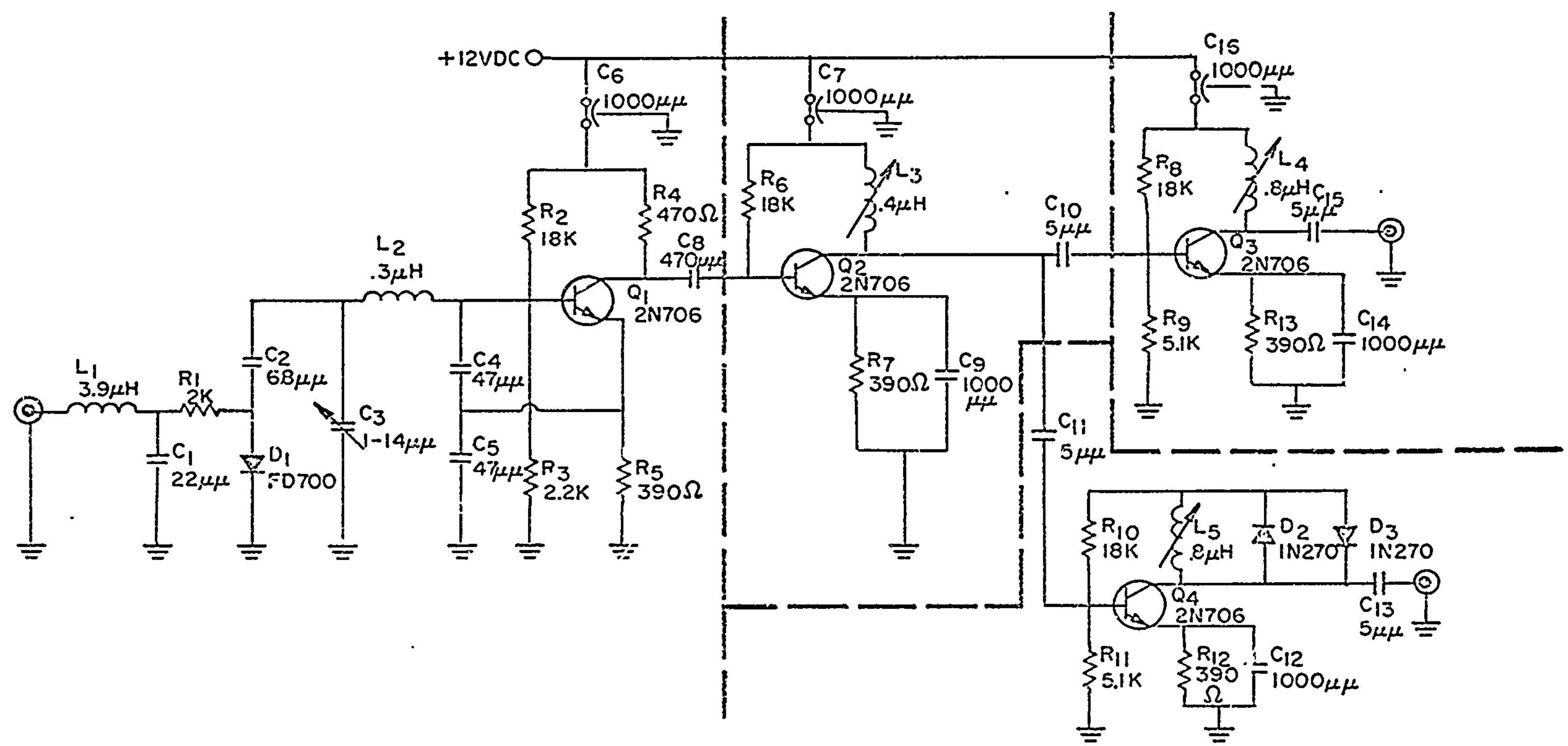

FIG. 3 - VOLTAGE CONTROLLED OSCILLATOR (VCO)

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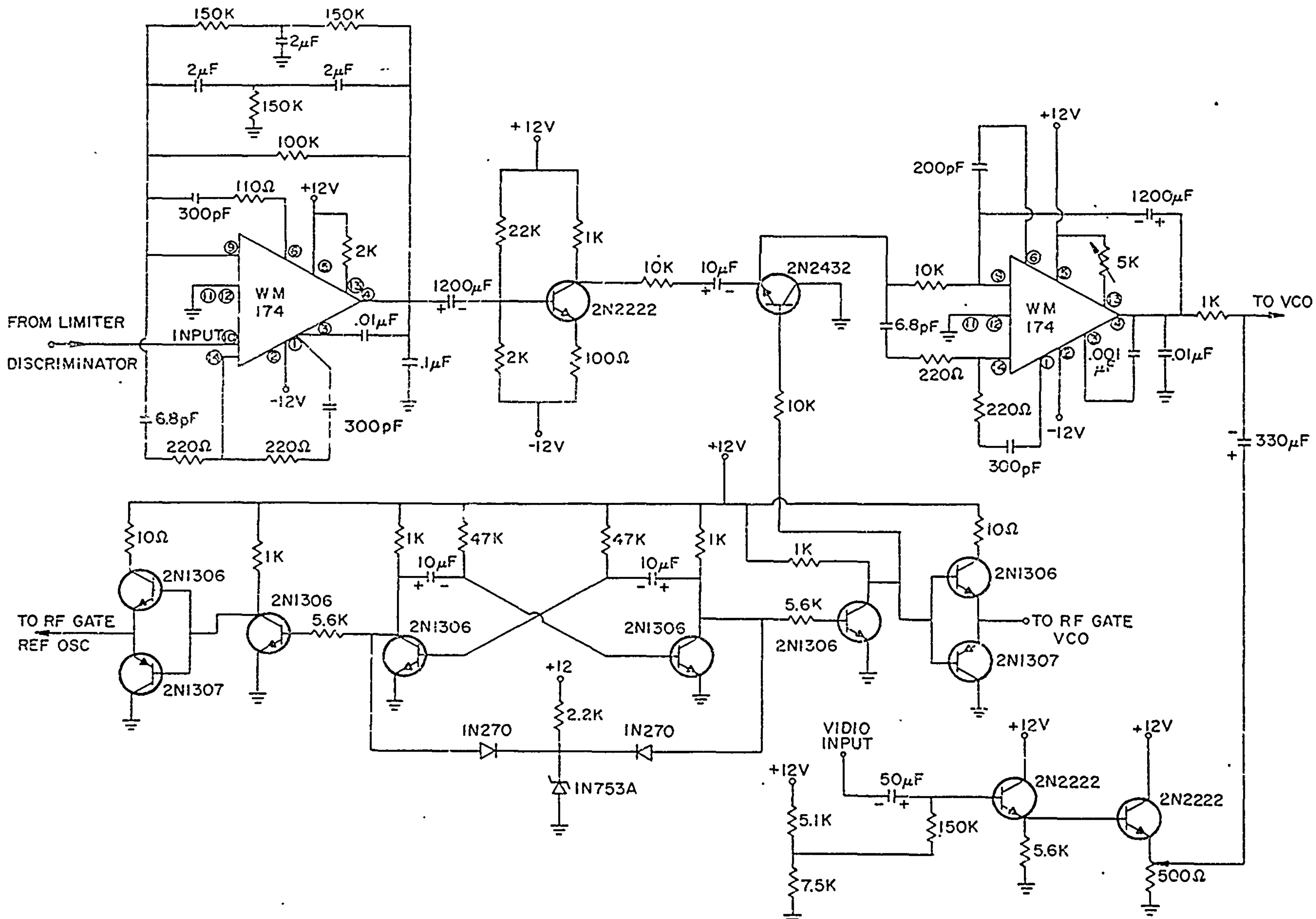

FIG. 4- SYSTEM AFC LOOP (0.5 Hz RATE)

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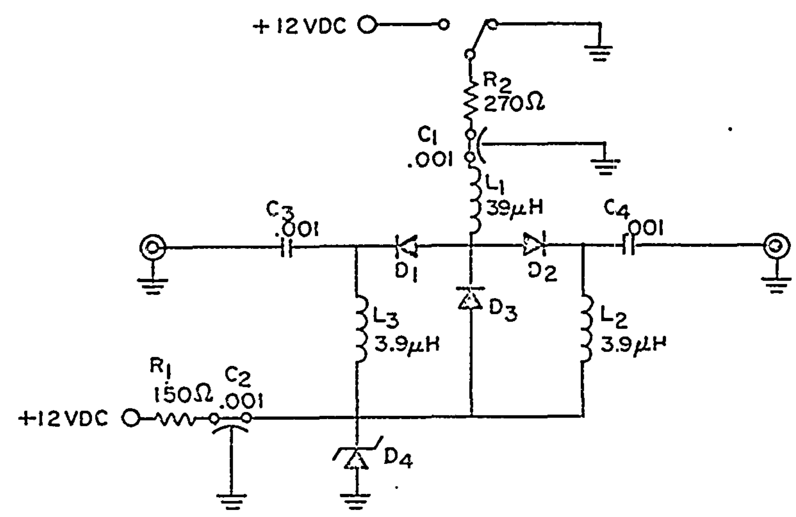

NOTE: D_1 D_2 & D_3 - FD700
D_4 - 1N753A

FIG. 5 - 81 MHz R.F. GATE

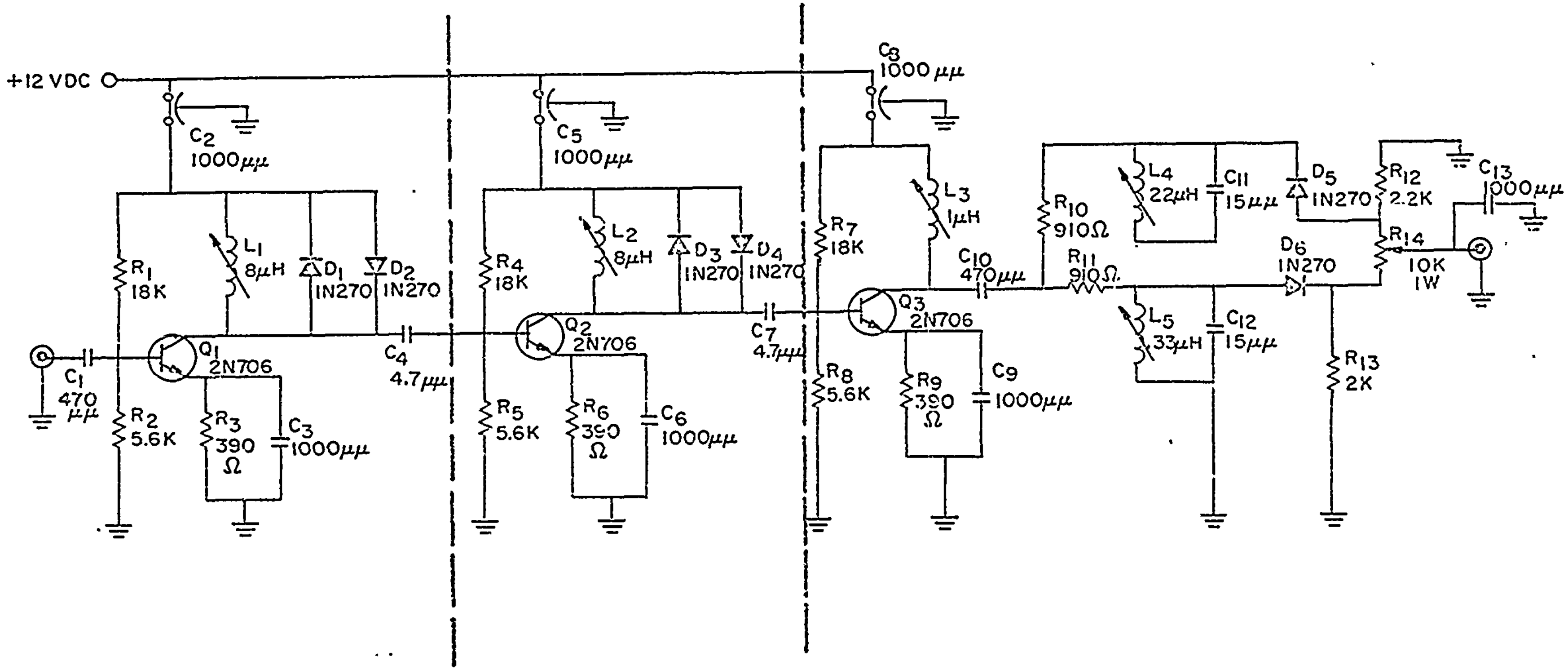

FIG. 6 – LIMITER DISCRIMINATOR CIRCUIT

This small error signal is then amplified in a narrow band a.c. amplifier incorporating a twin tee feedback circuit for stability and bandwidth control, (Since we are operating now only on the difference between the two signals, the long time stability of the discriminator circuit is not critical and zero drifts can be tolerated).

The amplified error signal is then phase and amplitude detected in a synchronous detector. This detector is of course driven by the same gating signal as the r.f. switches. The detected error signal, now having the proper d.c. direction, is next amplified. This stage is an operational amplifier used in a low frequency, d.c. coupled mode. Finally, the output of this stage is used as the stabilizing control for the VCO. The total loop gain is of the order of 90 dB.

In addition to this stabilizing signal, the video FM signal is also applied to the VCO through an isolating emitter follower stage. The video input is designed to have a 100 kΩ input impedance and produce a 1% frequency deviation with a 1 volt input.

Finally, the half of the VCO output which is not used in the AFC loop is applied to the multiplier and power amplifier stages through a buffer amplifier. In this final block, there is one amplifier stage followed by a times four multiplier. This multiplier stage uses the base to collector capacity of a 2N3553 transistor as a varactor multiplier.[1] The output of the multiplier is then passed through two stages of power amplification to produce a 324 MHz signal at approximately 9 watts. This signal is then used as input to the subsequent varactor multiplier stages. Details of this block are given in Figure 7.

[1] H.C. Lee and R. Minton, "Frequency Multiplication Using Overlay Transistors", R.C.A. Technical Publication ST-2989, Electronic Components and Devices, Harrison, N.J., 1965.

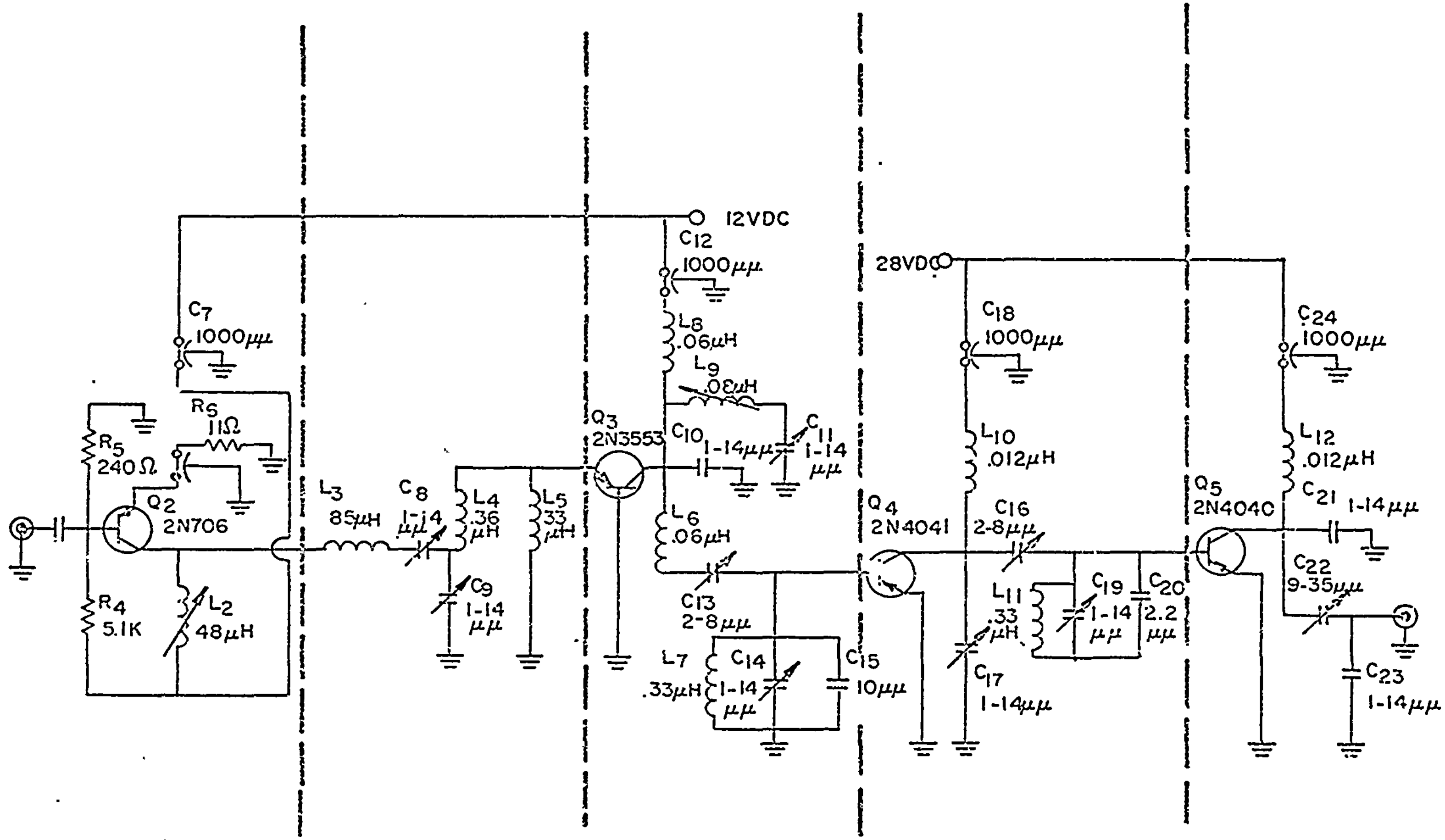

FIG. 7-MULTIPLIER AND DRIVER STAGE

3. VARACTOR MULTIPLIER CHAIN

The varactor multiplier portion of the 35 GHz solid state FM transmitter consists of five stages of multiplication as shown on the block diagram of Figure 8. Interstage isolation is provided between stages one and two and stages three and four by terminated circulators to improve the overall stability of the source. Between stages four and five, there is a miniature waveguide isolator, which was required to achieve stabilization across the desired bandwidth. Isolation of this nature improves performance since interface mismatches do not have as large a detrimental effect on the chain. Furthermore, use of the terminated port of a circulator as a test point (with an appropriate crystal detector replacing the load) allows monitoring of the impedance match into the succeeding stage during alignment.

In the first portion of the chain, step-recovery diodes (diodes exhibiting charge-storage) are used to give the best efficiency while providing good power handling capability. Silicon varactors with linearly graded junctions exhibit this charge-storage effect while gallium arsenide varactors have short recombination times and do not exhibit the effect. However, the higher cutoff frequencies available in gallium arsenide make their use preferable above 10 GHz.

In order to handle most efficiently the required power levels and the necessary impedance matching, the technique of stacking several varactors (in place of a higher breakdown voltage device) is utilized in some of the stages of the chain. This achieves a twofold purpose. First, the impedance levels of the multiplier are increased to levels more amenable to circuit transformations at low loss. Second, higher quality varactors can be used at power levels well above that for a single device since power handling goes up linearly as the number of varactors in the stack.

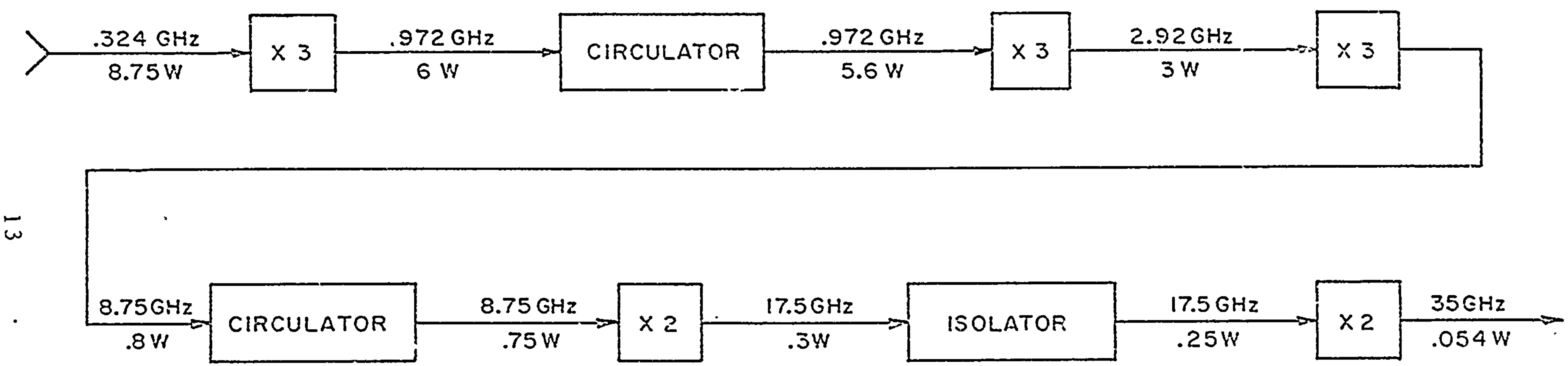

FIG. 8 - SOLID STATE FM TRANSMITTER VARACTOR MULTIPLIER CHAIN

Calculations of power handling, efficiency and impedance levels can best be described by the equations given in Figure 9 which may be found in "Varactor Applications" by Penfield and Rafuse. Extension of the derivations of the constants shown in these equations to cover charge-storage devices have been published by C. B. Burckhardt[2] of the Bell Telephone Laboratories. The constants tabulated in Figure 9 have been utilized in the choice of varactors for these multipliers.

Referring to the block diagram in Figure 8, the first tripler stage utilizes a single varactor, Motorola type IN5153. The theoretical input and output impedances are 62.6 and 10.4 ohms respectively (at the diode terminals). Theoretical output power is 6.5 watts. The configuration is a lumped circuit input and the idler with a tuned line output circuit. Self bias is used in this multiplier and throughout the chain is obtained by placing a resistor in shunt across the varactor. Measured output power is 6 watts with a circuit efficiency of 68.5% (See Figure 10).

The second tripler is isolated from the previous stages by a circulator required for maximum stability. This stage utilizes two Varian VAB804 varactors (in series) mounted in a shunt configuration in this multiplier. Theoretical conversion efficiency is 87% and the theoretical output power with infinite diode heat sink is 17.6 watts. Input and output impedances are 82.4 and 14 ohms respectively. The input and output circuits of this multiplier are coaxial cavities, with the idler tuned by a lumped circuit inductor and miniature variable capacitor. Measured output power from this stage was 3 watts at a circuit efficiency of 53.6%

[2] C. B. Burckhardt, "Analysis of Varactor Frequency Multipliers for Arbitrary Capacitance Variation and Drive Level", The Bell System Technical Journal, April, 1965, pp 675-692.

TABLE I - DOUBLER

	$\gamma = 0.0$		$\gamma = 0.333$			$\gamma = 0.4$			$\gamma = 0.5$	
Drive	1.5	2.0	1.0	1.3	1.6	1.0	1.3	1.6	1.3	1.6
α	6.7	4.7	12.6	8.0	6.9	11.1	8.0	7.2	8.3	8.3
β	0.0222	0.0626	0.0118	0.0329	0.0587	0.0168	0.0406	0.0678	0.0556	0.0835
A	0.117	0.213	0.0636	0.101	0.126	0.0730	0.102	0.118	0.0980	0.0977
B	0.204	0.211	0.0976	0.158	0.172	0.112	0.157	0.161	0.151	0.151
S_{01}/S_{max}	0.73	0.50	0.68	0.52	0.40	0.61	0.45	0.35	0.37	0.28
S_{02}/S_{max}	0.60	0.50	0.66	0.48	0.41	0.59	0.44	0.38	0.40	0.34
V_{0norm}	0.35	0.25	0.41	0.33	0.27	0.39	0.31	0.26	0.28	0.24

TABLE II - 1-2-3 TRIPLER

	$\gamma = 0.0$	$\gamma = 0.333$			$\gamma = 0.4$			$\gamma = 0.5$	
Drive	1.5	1.0	1.3	1.6	1.0	1.3	1.6	1.3	1.6
α	7.0	14.2	9.0	8.1	12.5	8.6	8.6	9.4	9.8
β	0.0212	0.0101	0.0281	0.0490	0.0144	0.0345	0.0563	0.0475	0.0700
P_{max}/P_{norm}	7.5×10^{-4}	1.8×10^{-4}	8×10^{-4}	1.4×10^{-3}	3.0×10^{-4}	9.6×10^{-4}	1.5×10^{-3}	1.2×10^{-3}	1.7×10^{-3}
ω_{0max}/ω_c	10^{-1}	7.0×10^{-2}	10^{-1}	10^{-1}	8.0×10^{-2}	10^{-1}	10^{-1}	10^{-1}	10^{-1}
A	0.185	0.104	0.170	0.214	0.120	0.172	0.200	0.168	0.172
B	0.0878	0.0471	0.0753	0.0871	0.0542	0.0755	0.0818	0.0728	0.0722
S_{01}/S_{max}	0.80	0.69	0.54	0.41	0.62	0.47	0.35	0.36	0.26
S_{02}/S_{max}	0.54	0.67	0.50	0.40	0.60	0.45	0.37	0.38	0.31
S_{03}/S_{max}	0.72	0.67	0.52	0.42	0.61	0.46	0.37	0.38	0.30
V_{0norm}	0.32	0.39	0.29	0.22	0.37	0.27	0.20	0.24	0.18

FIG. 9 - THEORETICAL PARAMETERS OF VARACTOR DIODES AS HARMONIC GENERATORS

MULTIPLIER		THEORETICAL VARACTOR VALUES		ACTUAL CIRCUIT VALUES	
No	Frequency	Power Out (watts)	Diode Efficiency	Power Out (watts)	Overall Circuit Efficiency
1	.324-972 GHz	6.5	92	6	68.5
2	.972-2.92 GHz	17.6	87	3	53.6
3	2.92-8.75 GHz	2.92	71	0.8	26.7
4	8.75-17.5 GHz	0.54	74	0.3	40.0
5	17.5-35.0 GHz	0.118	60	.054	21.6

FIG. 10 - COMPARISON OF THEORETICAL VALUES TO MEASURED VALUES FOR VARIOUS STAGES OF VARACTOR MULTIPLIER CHAIN

The third tripler stage utilizes two Varian VAB805 varactors in series, again shunt mounted. The input of this multiplier is a coaxial cavity with the idler being an open coaxial line tuned to resonance by varying the end capacitance of the line. The output of this stage is probe coupled and resonated into RG 51 waveguide. Theoretical output power is 2.92 watts at a theoretical efficiency of 71%. Impedance levels are 110 and 18.3 ohms respectively for input and output. Measured output power was 0.8 watts at a circuit efficiency of 26.7%. This stage in future models of such a multiplier chain should be redesigned as the circuit efficiency is poor and excessive losses are experienced, hence the chain's efficiency is below its optimum value.

A second isolator is used at this point to improve the stability of the chain. The fourth multiplier is a doubler and utilizes a single varactor, Sylvania type D5256B. Theoretical efficiency of this device is 74% and it can theoretically produce 0.54 watts of output power. Impedances are 9.7 and 13.3 ohms respectively. This multiplier is constructed in an inline configuration in waveguide. Measured circuit efficiency of this stage was 40% with 0.3 watts of output power.

Between this stage and the final doubler an isolator is required to maintain the necessary bandwidth. Without this isolator the necessary bandwidth is obtainable but the band flatness cannot be maintained.

The fifth stage is also a doubler and utilizes a single varactor, Sylvania type D5245D. This varactor theoretically can produce an output power of 118 milliwatts at 35 GHz. Theoretical conversion efficiency is 60% and input and output impedances are 13.8 and 18.4

ohms respectively. This stage is constructed similarly to the previous stage using an inline waveguide construction. Measured output power was 54 milliwatts at a circuit efficiency of 21.6%. One percent modulation caused the output power to drop to 48 milliwatts.

4. COMPLETED ASSEMBLY

The photograph of Figure 11 shows essentially all of the components of the final design. Only one circuit board is out of sight beneath the topmost chassis in the picture. On this chassis with the power supplies are the components described in Section 2.

Figure 12 shows perhaps more clearly the varactor multiplier chain. The 324 MHz signal comes up from the lower chassis to the first tripler. Then proceeding counterclockwise around the loop one encounters an isolator, the second tripler and the third tripler, another stage of isolation (using a 3-port circulator), a doubler, an isolator, and the final doubler to 35 GHz (more accurately, 34.992 GHz).

The finished package is shown in Figure 13. Operation of the unit is as simple as the front panel suggests: simply connect to 115 volt, 60 Hz, single phase power and turn on. Approximately 10 mintues of warm up time is required for the AFC circuit to be assured of an absolute lock on the crystal oscillator. The r.f. power however, well in excess of the specified 25 mW, is available immediately.

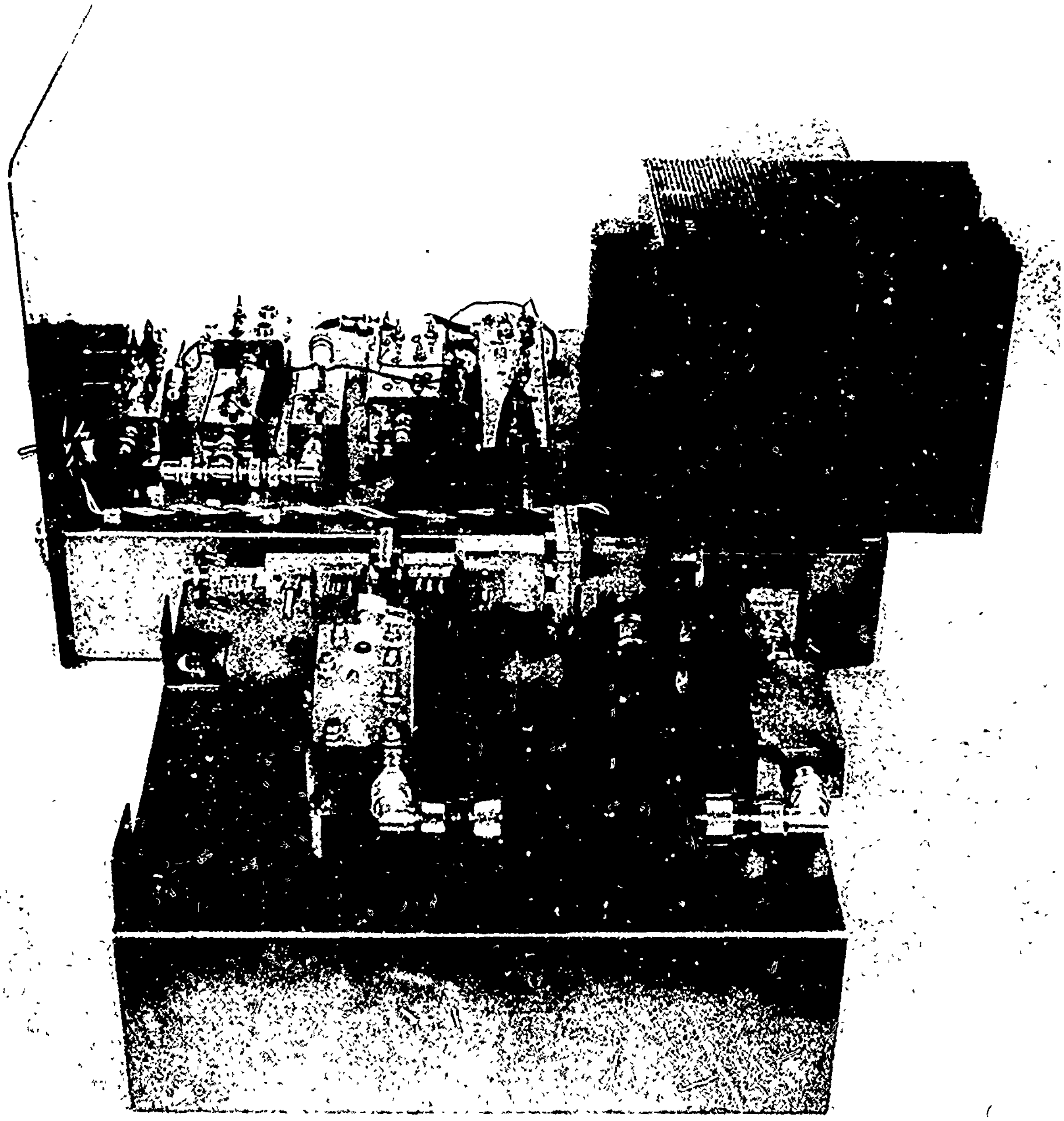

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Fig. 11 - Disassembled View of Source

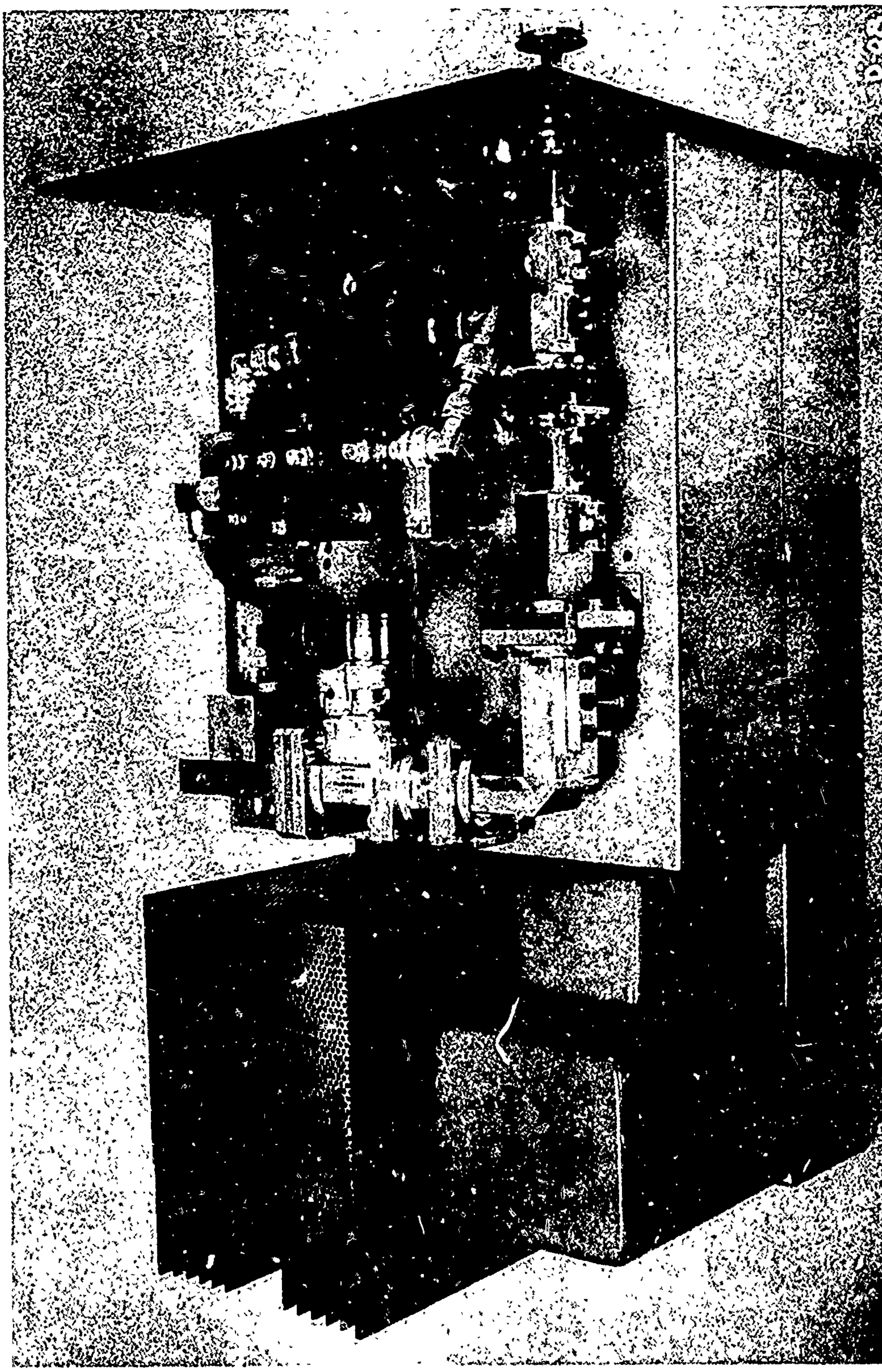

Fig. 12 - Assembled View of Source

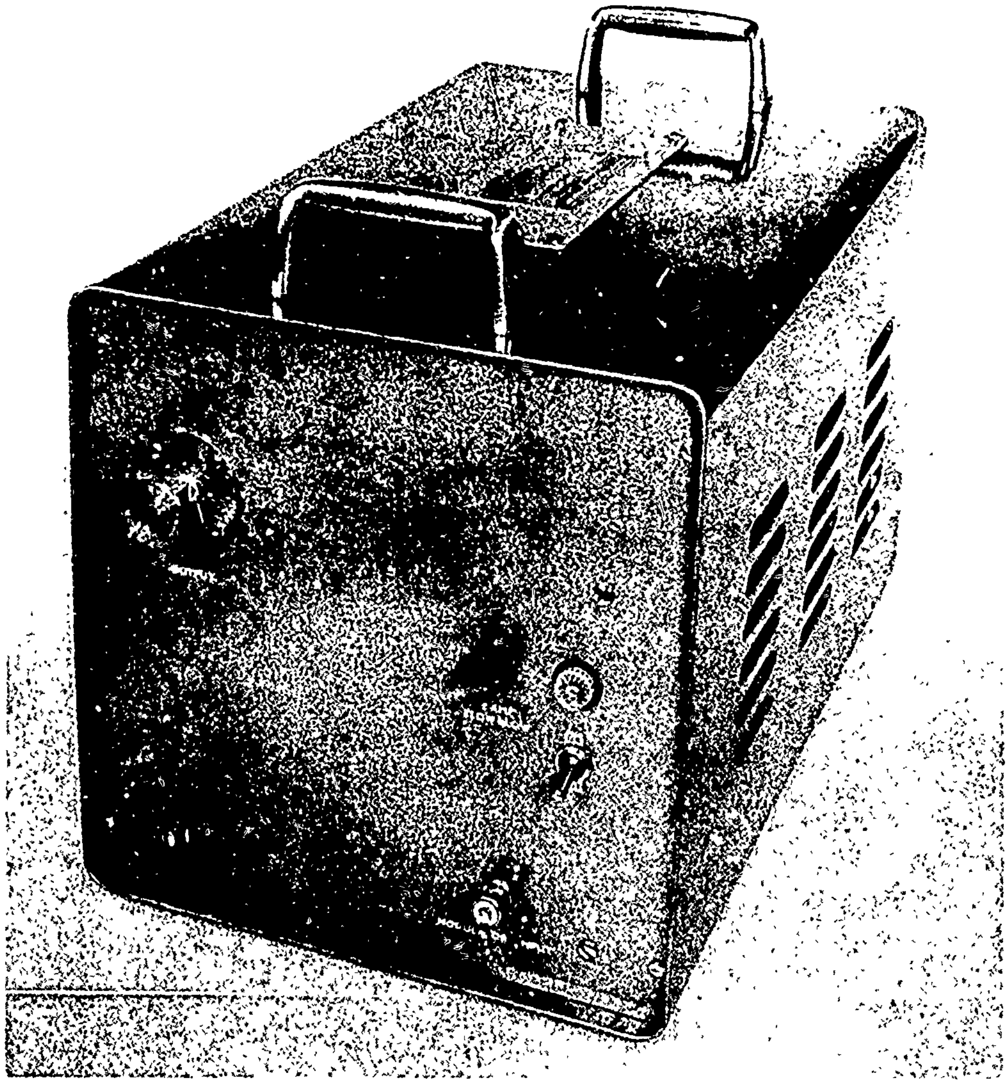

Fig. 13 - Completed 35 GHz Package

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13. ABSTRACT

This report describes the design of a 35 GHz solid state source. A unique feature of the source is a linear FM capability of 350 MHz at sweep rates from 5 Hz to greater than 20 kHz. The output power is approximately 50 mW. Frequency stability is derived from an 81 MHz crystal controlled oscillator. Transistor circuitry brings this signal up to 324 MHz at 9 watts. A varactor multiplier chain then is used to achieve the final output frequency.

This source was developed as one of several work assignments of the subject contract.

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